WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

an input/output (I/O) pad;

an interface circuit connected to said I/O pad; and

a charged device model (CDM) clamp circuit connected to said pad and to said interface circuit, wherein said CDM clamp circuit and said interface circuit are adjacent to each other and share a common device element.

2. The integrated circuit of claim 1, further comprising a resistor disposed between said I/O pad and said interface circuit.

3. The integrated circuit of claim 1, wherein said CDM clamp circuit comprises a first transistor and said interface circuit comprises a second transistor.

4. The integrated circuit of claim 3, wherein said first and second transistors are MOS transistors.

5. The integrated circuit of claim 4, wherein said CDM clamp circuit and said interface circuit share a common source region.

6. The integrated circuit of claim 1, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

7. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

8. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

9. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

10. A method of protecting an integrated circuit from electrostatic discharge (ESD), said integrated circuit comprising an input/output (I/O) pad and an interface circuit connected to said I/O pad, said method comprising:

disposing a charged device model (CDM) clamp circuit adjacent to said interface circuit and connected to said pad and to said interface circuit; and

sharing a common device element between both said CDM clamp circuit and said interface circuit.

11. The method of claim 10, wherein said CDM clamp circuit comprises a first MOS transistor and said interface circuit comprises a second MOS transistor.

12. The method of claim 11, wherein said common device element is a source region.

13. The method of claim 10, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

14. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

15. The method of claim 13, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

16. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

17. An integrated circuit comprising:

a semiconductor substrate;

a first drain region disposed in said substrate;

a first channel region disposed in said substrate directly adjacent to said first drain region;

a first gate dielectric overlying said first channel region;

a first gate overlying said first gate dielectric;

a first source region disposed in said substrate directly adjacent to said first channel region;

a second channel region disposed in said substrate directly adjacent to said first source region and on a side of said first source region opposite to said first channel region;

a second gate dielectric overlying said second channel region;

a second gate overlying said second gate dielectric; and

a second drain region disposed in said substrate directly adjacent to said second channel region.

18. The integrated circuit of claim 17, further comprising an input/output pad electrically coupled to said first gate and to said second drain region.

19. The integrated circuit of claim 17, wherein said substrate is p-type, and wherein said source and drain regions are n+ regions.

20. The integrated circuit of claim 17, further comprising an n-well disposed in said substrate around said regions, wherein said substrate is p-type, and wherein said source and drain regions are p+ regions.

21. A method of forming an integrated circuit, said method comprising:

forming a first drain region in a semiconductor substrate;

forming a first source region in said substrate separated from said first drain region solely by a first channel region;

forming a second drain region in said substrate separated from said first source region solely by a second channel region, wherein said second channel region is a different region than said first channel region;

forming a first gate dielectric overlying said first channel region and a second gate dielectric overlying said second channel region; and

forming a first gate overlying said first gate dielectric and a second gate overlying said second gate dielectric.

22. The method of claim 21, further comprising forming an input/output pad on said semiconductor substrate electrically coupled to said first gate and to said second drain region.

23. The method of claim 21, wherein said substrate is p-type, and wherein said source and drain regions are n+ regions.

24. The method of claim 21, further comprising forming said source and drain regions in an n-well in said substrate, wherein said substrate is p-type, and wherein said source and drain regions are p+ regions.